Reconfigurable VLSI Communication Processor Architectures

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12 August 2002 – Futura Workshop
Goals of Reconfigurable VLSI Processor Architectures for 4G Systems

- Seamless Hardware/Software Integration of Many Individual Wireless Services
  - Cellular Radio (W-CDMA, GPRS, EGPRS)
  - WLAN (802.11a & 802.11b)
  - PAN (Bluetooth)
- High Data Rate Heterogeneous Connectivity
- Low-Power and Flexible Performance Modes
- WindMill and RENÉ (Rice Everywhere NÉtwork) Projects
Network Architectures

- Backbone Network
- Proxy
- Proxy
- Proxy
- Wired LAN
- Wireless Cellular
- Wireless LAN
- Home area network
  - Ubiquitous
  - Single Hardware
  - Reconfigurable
Power-Efficient VLSI/DSP Architectures - WindMill

- Power-Aware Detector Implementations
- Real-Time Reconfigurable Decoder Implementations
- Hardware/Software Partitioning – DSP/FPGA/ASIC
- RF Power Amplifier Control
Rice Reconfigurable Baseband Concept

RF interface → Home WLAN
RF interface → Cellular W-CDMA
RF interface → Office HS WLAN

Base Band
DSP
FPGA
ASICS

Mobile Host
Current Projects and Research Directions

- Embedded Systems for Wireless Communication System Design Exploration
- Reconfigurable Accelerators for Multiple Standards and Systems
- RF Radio Testbed Architectures for End to End System Evaluation
Embedded Systems Evaluation Platform

900 MHz Linx or 2.4 GHz Welkin Radio

Reconfigurable, Expandable Testbed Lyr Signal Master System

A/D DAC

Xilinx FPGA

TI C6701 DSP

Host CPU
Hardware Software Co-Design Objectives

- DSP / FPGA Design Partitioning using Lyr Signal Processing Signal Master
- Simulink Control of DSP FPGA and A/D D/A converters
- “Wrapper” and “Switcher” Tools Allow for Integration of “C” code into Simulink and Selection of Host or DSP Execution
- Support Xilinx System Generator for High-level FPGA Programming
Simulink Model for Transmitter
High Level Control and Co-execution
Embedded System Platform for Wireless Communications

- Lyr Signal Processing
- TI C67 Floating-Point DSP
- Xilinx FPGA
- Simulink control of both DSP and FPGA
- Baseband Algorithms
- Performance Evaluation
- Interface to A/D D/A for W-CDMA, WLAN
Opportunities for Reconfigurable Accelerators for Communication Systems

- Commonality of Algorithms, e.g. Viterbi Decoder,
  - WLAN – Rate \( \frac{1}{2}, \frac{2}{3}, \frac{3}{4} \), Constraint Length 7
  - W-CDMA – Rate \( \frac{1}{2}, \frac{1}{3} \), Constraint Length 9
- Adaptation – Coarse Grain Reconfigurable FPGA’s
  - Chameleon Systems
  - PACT Corp
- Configurable Processors
  - Examples: Stanford IMAGINE, MIT RAW, Univ. Washington RaPiD
  - Functional Units to Suit Application
Viterbi / Turbo Reconfiguration Potential

- Turbo decoding architecture using SOVA-based Viterbi blocks
Viterbi / Turbo Power Consumption

- Xilinx Virtex-2 Design
- Modelsim and Xilinx Xpower Analysis
- Variable Data Rates and Constraint Lengths Affect Complexity

<table>
<thead>
<tr>
<th>Decoder Type</th>
<th>Clock Frequency</th>
<th>Data Rate</th>
<th>Power Consumption (excluding Quiescent Power)</th>
<th>Quiescent Power</th>
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</thead>
<tbody>
<tr>
<td>Viterbi (K=5)</td>
<td>54 MHz</td>
<td>54 Mbps</td>
<td>138.06 mw</td>
<td>225 mW</td>
</tr>
<tr>
<td>Viterbi (K=5)</td>
<td>2 MHz</td>
<td>2 Mbps</td>
<td>5.11 mw</td>
<td>225 mW</td>
</tr>
<tr>
<td>Viterbi (K=7)</td>
<td>54 MHz</td>
<td>54 Mbps</td>
<td>501.3 mw</td>
<td>225 mW</td>
</tr>
<tr>
<td>Viterbi (K=7)</td>
<td>2 MHz</td>
<td>2 Mbps</td>
<td>18.5 mw</td>
<td>225 mW</td>
</tr>
<tr>
<td>Viterbi (K=9)</td>
<td>54 MHz</td>
<td>54 Mbps</td>
<td>1.42 w</td>
<td>225 mW</td>
</tr>
<tr>
<td>Viterbi (K=9)</td>
<td>2 MHz</td>
<td>2 Mbps</td>
<td>59.54 mw</td>
<td>225 mW</td>
</tr>
<tr>
<td>Turbo</td>
<td>54 MHz</td>
<td>3.15 Mbps</td>
<td>165.02 mw</td>
<td>225 mW</td>
</tr>
<tr>
<td>Turbo</td>
<td>34.3 MHz</td>
<td>2 Mbps</td>
<td>104.76 mw</td>
<td>225 mW</td>
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</table>
WCDMA Rake Receiver Architectures and Implementation Tradeoffs

- Power optimization potential: wordlength scaling, sample rate variation, clock gating...
- Case study: Virtex-2 FPGA based design with 3 Rake fingers
WCDMA Rake Receiver Architectures

- Power optimizations based on wordlength
- Modelsim and Xpower analysis with Matlab precision calculations

<table>
<thead>
<tr>
<th>Wordlength (bits)</th>
<th>Area (CLB Slices)</th>
<th>Slice Flip-flops</th>
<th>4 Input LUT*s</th>
<th>Dynamic Power (mW) (Static Power:225 mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>3572</td>
<td>6366</td>
<td>5847</td>
<td>69.22</td>
</tr>
<tr>
<td>14</td>
<td>3000</td>
<td>5301</td>
<td>4583</td>
<td>66.31</td>
</tr>
<tr>
<td>12</td>
<td>2341</td>
<td>4075</td>
<td>3475</td>
<td>63.09</td>
</tr>
<tr>
<td>10</td>
<td>1862</td>
<td>3185</td>
<td>2529</td>
<td>59.89</td>
</tr>
</tbody>
</table>
## Programmable Communication Architectures for Wireless Systems

<table>
<thead>
<tr>
<th>Processor Type</th>
<th>Algorithms</th>
<th>Data rate targets</th>
<th>Constraints</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobile</td>
<td>W-CDMA, W-LAN</td>
<td>1Mbps, 100Mbps/#users</td>
<td>Time, Power, Area</td>
</tr>
<tr>
<td>Base-station</td>
<td>W-CDMA</td>
<td>4 Mbps</td>
<td>Time, maybe area</td>
</tr>
<tr>
<td>Base-station</td>
<td>W-LAN</td>
<td>100 Mbps</td>
<td>Time, maybe area</td>
</tr>
</tbody>
</table>

### Performance vs. Flexibility

- GPP
- DSP
- FPGA
- VLSI

Best architecture for Power, Area constraints ????
Communication Architecture Design Issues

- Cycle accurate simulation and compiler technology for design exploration:
  - GPP simulators: RSIM, SimpleScalar
  - VLIW multi-cluster: IMAGINE

- Example: Stanford IMAGINE architecture has VLIW-based multiple functional unit cluster

- Multiple functional unit and cluster extensions and organization

- Custom functional unit extensions – MMX-like
The IMAGINE Architecture

Imagine Stream Processor

Stream Register File

Streaming Memory System

Network Interface

Host Processor

Microcontroller

ALU Cluster 0

ALU Cluster 1

ALU Cluster 2

ALU Cluster 3

ALU Cluster 4

ALU Cluster 5

ALU Cluster 6

ALU Cluster 7
RF Radio Testbed Architectures for End-to-End System Evaluation

Radio Module
RF Micro Devices & Custom Welkin Radio
2.4 GHZ
(M. Fitz & U. Mitra)

Connect to DSP via A/D D/A

W-CDMA and WLAN physical layer
Rice 2.4 GHz Custom Radio Link Testbed
Radio Testbed Experiments

- Linx 900 MHz and Welkin 2.4 GHz Testbeds
- Spirent TAS Channel Emulator for WCDMA and WLAN Testing
- WLAN 802.11b and Bluetooth Range Studies
- Campus Shuttle Bus Mobile Bluetooth/GPS Platform
Radio Testbed Performance Experiments

Space Time Coding Configuration

Multiuser Detection Configuration
Rice Wireless Integrated Network Device (WINDS)

- “Proof-of-Concept” Hardware for a Multitier Network Interface Device (mNIC)
- Built from Common Off-the-Shelf Components (COTS)
- Currently Functioning and Being Deployed on Rice University Campus
WINDS Block Diagram

- Axis ETRAX 100LX Linux Microprocessor
- Class 1 Bluetooth Module
- 802.11a or 802.11b PC Card (In Progress)
- 10/100 Wired Ethernet Port
- GPS Receiver

GPP Host
Axis
ETRAX LX100
Linux SoC

- Bluetooth Module
- 802.11b PC Card
- Wired 10/100 Ethernet
- GPS Receiver
The WINDS Prototype

GPS

Bluetooth

PLD/FPGA

USB

Wired Ethernet
WINDS Future Plans

- Finish Integration of 802.11
- Integrate Custom W-CDMA Radio for Wide Area Cellular & Baseband Algorithm Experiments
- Implementation of Various Ad Hoc Routing Protocols
Rice University Shuttle Bus Project (RUSH)

- Deployment platform for WINDS & Other Projects
- Administration Agrees to Let Us Place Custom Hardware on Shuttle Bus System
- Provides a “Real-World” and mobile Environment to Test Our Prototypes
RUSH Topography

- Currently Beginning Deployment Throughout Campus
- 4 “Basestations”
- 8 Mobile Terminals (On the Busses)
Summary and Future Directions

- System Architecture and Implementation
  - W-CDMA, WLAN, Bluetooth, etc…
- Physical Layer
  - Baseband - Reconfigurable DSP / FPGA Design
  - IMAGINE-like Communications Processor
  - RF – 2.4GHz Radios End-to-End Testbed
- Low-Power Design Methodology
- Multiple Antenna Systems