ANATOMY OF THE SINGLE CHIP PHONE

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SINGLE CHIP PHONE

AGENDA

• Moore’s Law Scaling
• Design for Low Power
• SOC Integration of Analog/RF Functions
• Digital Radio Processor
• LoCosto!!
Semi-Conductor Scaling

35 Years of Scaling History

- Every generation
  - Feature size shrinks by 70%
  - Transistor density doubles
  - Wafer cost increases by 20%
  - Chip cost comes down by 40%

- Generations occur regularly
  - On average every 2.9 years over the past 35 years
  - Recently every 2 years

Modern CMOS
Beginning of Submicron CMOS
Deep UV Litho
90 nm in 2004
65 nm in 2006
Presumed Limit to Scaling
## GSM Digital Baseband Evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Die size (mm²)</th>
<th>Dies per wafer</th>
<th>Wafer size</th>
<th>Nanometer</th>
</tr>
</thead>
<tbody>
<tr>
<td>1994</td>
<td>80.7</td>
<td>310</td>
<td>6&quot;</td>
<td>500nm</td>
</tr>
<tr>
<td>1997</td>
<td>46.6</td>
<td>950</td>
<td>8&quot;</td>
<td>350nm</td>
</tr>
<tr>
<td>1999</td>
<td>19.2</td>
<td>2550</td>
<td>8&quot;</td>
<td>250nm</td>
</tr>
<tr>
<td>2000</td>
<td>10.7</td>
<td>4700</td>
<td>8&quot;</td>
<td>180nm</td>
</tr>
<tr>
<td>2002</td>
<td>6.7</td>
<td>12,200</td>
<td>12&quot;</td>
<td>130nm</td>
</tr>
<tr>
<td>2004</td>
<td>4.2</td>
<td>18,700</td>
<td>12&quot;</td>
<td>90nm</td>
</tr>
<tr>
<td>2006</td>
<td>2.4</td>
<td>26,500</td>
<td>12&quot;</td>
<td>65nm</td>
</tr>
<tr>
<td>2008</td>
<td>1.4</td>
<td>46,500</td>
<td>12&quot;</td>
<td>45nm</td>
</tr>
</tbody>
</table>

150X increase in die per wafer
First 65 nm Product: DBB chip

Features:
• Die Size: 13.3mm²
• 5.9M bits SRAM
• 1.9M gates of logic
  ➢ eFuse (dieID) and repair
  ➢ ARM7 uC
  ➢ LEAD3 DSP (250K gates)
  ➢ MegaCell (300K gates)
  ➢ ASIC gates (1.3M gates)
• Volume Production
65 nm Features

- Logic density: > 2x 90nm, 930k gates/mm\(^2\)
- SRAM memory density: > 2x 90nm, 1400k bits/mm\(^2\)
- Active power reduction: > 40% of 90nm
- Leakage power reduction: > 1000x of 90nm
- Performance: 15% higher than 90nm
- Ni Silicide
- Strain: PMD liner & Capped Poly
- (100) Si
- \(k_{\text{eff}}\) from 3.55 @ 90 nm to 3.31
Lithography

Year of Production

Resolution (μm)

Above Wavelength

1980 1990 2000 2010

Near Wavelength

1980 1990 2000 2010

Below Wavelength

1980 1990 2000 2010

Above Wavelength

Resolution (μm)

Near Wavelength

Below Wavelength

Wavelength

g-line λ = 436nm

i-line λ = 365nm

DUV λ = 248nm

i-line λ = 193nm

i-193 λ′ = 133nm

EUV λ = 13.5nm

10 1

0.1

0.01

0.001

0.0001

0.00001

0.000001

0.0000001

0.00000001

0.000000001

0.0000000001

0.00000000001

0.000000000001

0.0000000000001
STRUCTURED LAYOUT (45 nm)

- Vertical poly gates only
- GHOST Poly
- Poly not required to overlap contact
- Max Xstor width change within ACTIVE
TI CMOS Roadmap
Issues/Trends

• Relentless focus on power reduction.
• Design for Manufacturing Variations
• Analog/RF SOC Integration
• Co-Development of Process, Design techniques and Architecture
• CMOS processes customized to the application
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Deep Submicron Processes Demand Enhanced Power Management

Talk Time: \( \text{Pwr\_Active} = CV^2F + \text{Leakage} \)
- C: Decrease/node, offset by complexity
- F: Increases/node
- Leakage: Increases/node, temp.

Standby Time: \( \text{Pwr\_Idle} = \text{Leakage} \)
- Leakage: Increases/node, temp

**Technology: memory Iddq**

![Graph showing increasing Iddq for different technology nodes.](image)

**Memory Iddq vs. Power Management**

![Another graph showing Iddq comparison with and without PM.](image)
Power Domain Partitioning

- **Main Power Domains**
  - DSP
  - Data Memory
  - Modem Logic

- **Others**
  - Power Mngmt Control
  - MCU
  - DPLL
  - Analog
  - IO
Approaches to Power Reduction

VDD for IO = 1.8V

VDD Core: ~1.0V in retention

LDO (0.5V)

VSS (0V)
Memory Retention

- **Active Mode**
  - Periphery On
  - VSSM = 0V
  - VDD = V Nominal

- **Retention**
  - Periphery Off
  - VSSM ~ 0.5V
  - VDD ~ 1.0V
Silicon Measurements

Cumulative Yield

Iddq at Room Temperature

With Power Management

Without Power Management

Reduction: ~30X
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Why Single-Chip Phone?

• "Integration is like gravity"
  – Already happened in hard-disk drives, ADSL, etc
  – Not a single example of reversal
• “$20 phones”
• Large untapped market in India and China
• More “real estate” space for advanced features
• Better reliability
  – Today, more than half of the total components on a board are analog RF components
• Longer talk time
Typical Cell-Phone Block Diagram

Area and cost must be reduced → integrate!
What about SiP Integration?

- Monolithic integration of DRAM would result in significant cost increase due to the need for additional mask levels.
- Memory modules are highly reusable so modularity makes sense.
- No yield impact issue due to in-package integration of memory.
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Conventional Transceivers

- RF transmitters in commercial wireless applications are traditionally based on charge-pump PLL's and IQ upconversion mixers
- RF receivers use continuous-time mixing, filtering and amplification
- Design flow and circuit techniques are analog intensive
- Technology incompatible with modern digital processors
  - Low-voltage deep-submicron CMOS
DRP RF Architecture

0.2, 1.25, 2.5, 5, 10, 15, 20MHz BW
450, 800, 900, 1800, 1900, 2100, 2500, 3400MHz Transmission bands
GMSK, QPSK, 8-PSK, 16QAM, 64QAM Modulation
TDMA, FDMA, CDMA, OFDMA, IFDMA schemes
Looks like SDR!!
DRP/SoC Proven in Many Products

1/2 the silicon
1/2 the power
1/2 the board area

BlueLink™
Bluetooth

NaviLink™
A-GPS

WiLink™
Wi-Fi

Hollywood™
mDTV

“LoCosto”
GSM/GPRS

More to come…
**Single-Chip GSM Radio**

- 90 nm CMOS
- All-digital PLL
- All-digital TX
- Digitally-intensive RX
- w/o
  - 2-W PA
  - Battery management
New Paradigm

In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of an analog signal.
Deep-Submicron CMOS Rules

• **Exploit:**
  – Fast switching characteristics of MOS transistors
  – Small device geometries and precise device matching
  – High density of digital logic: 250 kgates/mm² in 90-nm CMOS
  – High density of SRAM memory: 1 Mbits / mm² in 90-nm CMOS

• **Avoid:**
  – Biasing currents for analog circuits
  – Reliance on voltage resolution
  – Nonstandard devices not needed for memory and digital logic
Multi-Disciplinary Technology

System Architecture
(GSM, Bluetooth, WLAN, mDTV)

Circuit Design
(LNA, ADPLL, DAC, ADC, Logic)

Silicon Process Technology
(90nm, 65nm, 45nm digital RF processes)

Manufacturing Expertise
(300mm, self-test, DD limited yield)

DRP

65nm transistor

300mm
Digital Radios Offer Many Benefits

Why Digital?

- **Process Capability**: We can now clock systems at radio frequencies
- **Entitlement**: Digital technology takes advantage of advanced logic capability (and leverages the wafer process technology investment)
- **Node Migration**: Digital systems scale with lithography and are easy to migrate
- **Performance**: Performance improves with new technology, the job keeps getting easier
- **Cost**: Digital radios offer excellent performance, low power consumption, high manufacturing yield, and low cost
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LoCosto – First Single-chip Phone

- Includes all major phone functions, supports quad-band GSM/GPRS
  - DBB logic
  - SRAM
  - Analog – A/D, D/A, misc.
  - Power Mgmt - Regulators
  - RF – Transceiver

- Advanced Process Technology
  - 90nmCMOS
  - No “extra” reticles or steps

- Advanced Manufacturing
  - BIST – low cost testing
  - Digital techniques - high yield
SoC Drives Cost Reduction

- SoC Integration Includes:
  - Digital baseband
  - SRAM
  - Power management
  - Analog
  - RF
  - Processors & Software

- The DRP technology enables digital implementation of traditional analog RF functions in standard CMOS

- Most advanced process technology used to maximize integration while minimizing cost
  - 90nm (shipping)
  - 65nm (mature design)
  - 45nm and beyond (preliminary)
Technology in the Internet Age

Moore’s Law is predicted to stagnate toward the end of the next decade ...
Technology in the Internet Age

Moore’s Law is predicted to stagnate toward the end of the next decade ...

... but SOC Integration has the potential to continue IC cost reduction and to perpetuate growth of Personal Internet Products.
Thank you