VLSI Architectures and Rapid Prototyping Testbeds for Wireless Systems

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Outline

- ***Rice University CMC and University of Oulu CWC***
- Wireless Systems Evolution
- Baseband Processor Challenges
- Application Specific Architectures
  - ⇒ Imagine Media Processor
  - ⇒ Transport Triggered Architectures
- Testbed Systems
  - ⇒ LabVIEW FPGA, Xilinx System Generator
  - ⇒ Rice CMC Testbed
  - ⇒ Oulu CWC Elektrobit 4G Testbed
- Summary

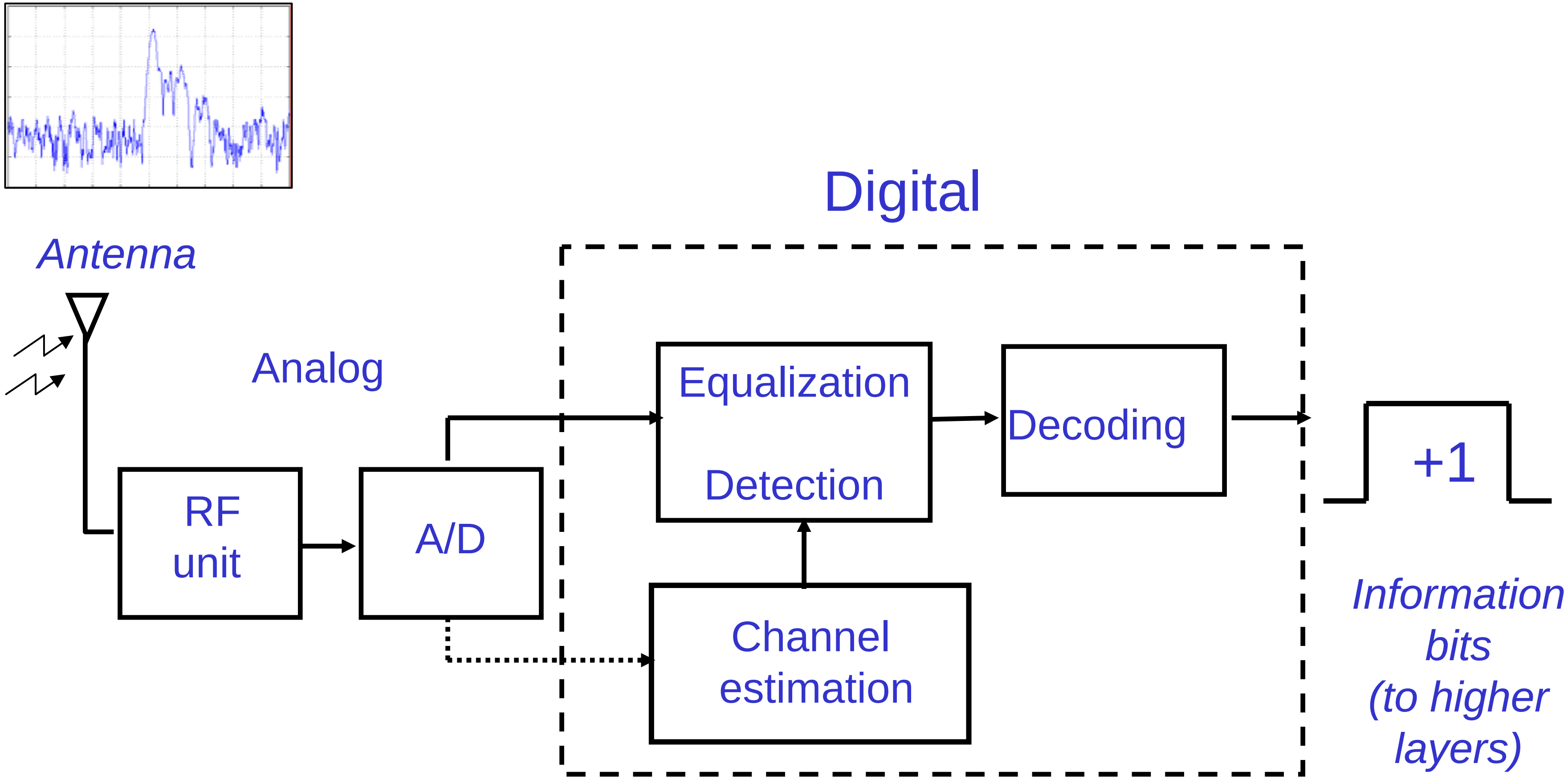
Rice CMC and University of Oulu CWC Interaction

- ❐ Rice CMC and Oulu CWC Common Vision on Wireless Systems
  - ⇒ Algorithms, Architectures, Testbeds
  - ⇒ Communications, VLSI, Networks
- ❐ Faculty and Student Exchange and Courses
  - ⇒ Wireless Systems Architecture
    - Parallelism and FPGA Prototyping
- ❐ Research Interaction
  - ⇒ WCDMA and WLAN Systems
  - ⇒ Beyond 3G Systems with TI and Nokia
- ❐ Nokia Foundation Fellowship – Spring 2005

Wireless Communication Architectures

- ❒ Cellular Generation Evolution from 2G to 4G
  - ⇒ 4G (MC-CDMA/OFDM) Voice & 100 Mbps Data…
- ❒ Wireless LAN Evolution
  - ⇒ 11 Mbps, 54 Mbps (802.11a,b,g), 100 Mbps….
- ❒ VLSI Signal Processing Architectures are the Key
  - ⇒ Algorithms to Architectures
  - ⇒ DSP, ASIP, or ASIC
  - ⇒ Theory and Experimentation

Communication System – Physical Layer Receiver



Digital

Antenna

Analog

RF unit

A/D

Equalization

Detection

Decoding

Channel estimation

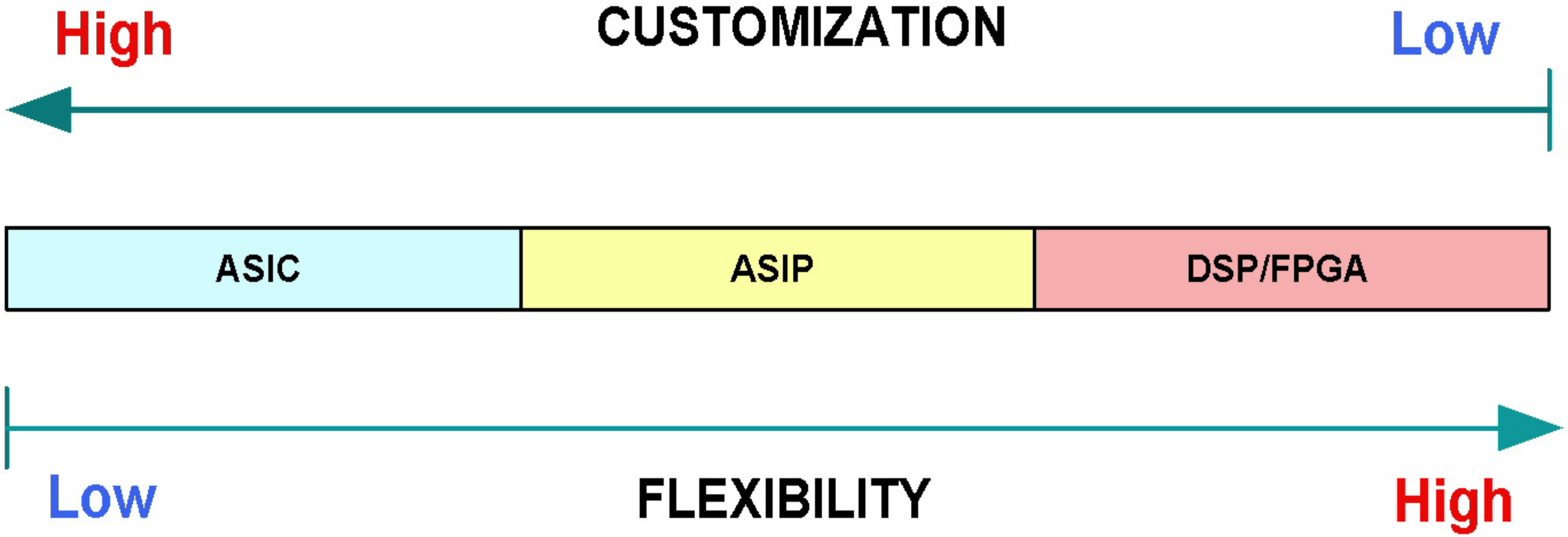
+1

Information bits (to higher layers)

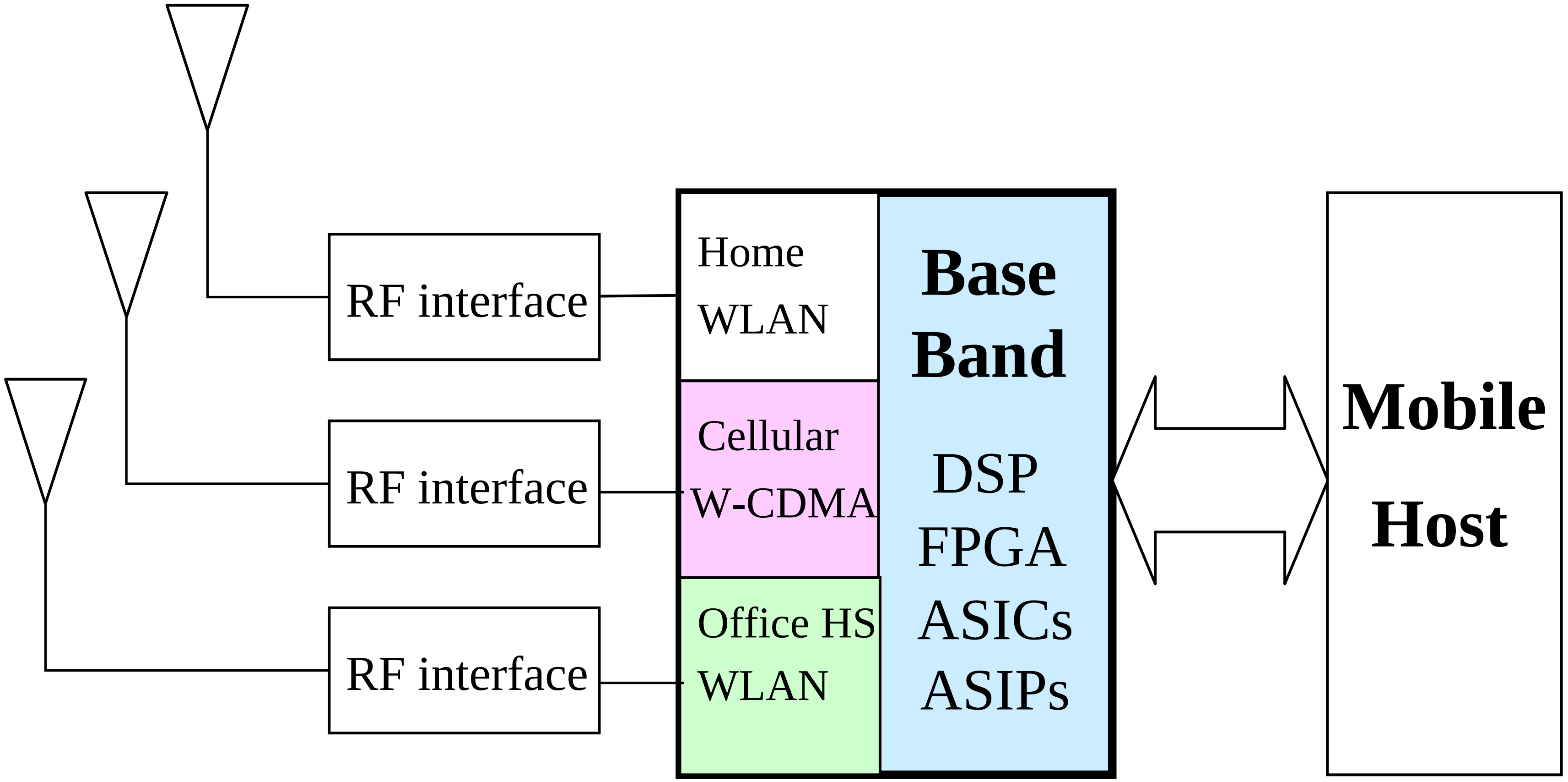
MIMO Research Challenges

- Communication Algorithms – Coding Strategies
- High Complexity Real-time Signal Processing –
  - ⇒ VLSI, FPGA, Application Specific Processors
  - ⇒ Reconfigurable Accelerators for Multiple Standards
- Network Scheduling – Transit Access Points
  - ⇒ Multiple RF Interfaces
- Experimentation and Verification with Real-Time RF Hardware in CMC Lab
  - ⇒ Behnaam Aazhang, Ashutosh Sabharwal, Patrick Frantz, Edward Knightly, Richard Baraniuk
- Contributions by: Sridhar Rajagopal, Predrag Radosavljevic, Marjan Karkooti, and Patrick Murphy

Challenges of Customization and Flexibility



Reconfigurable Baseband Architectures



RF interface

RF interface

RF interface

Home WLAN

Cellular W-CDMA

Office HS WLAN

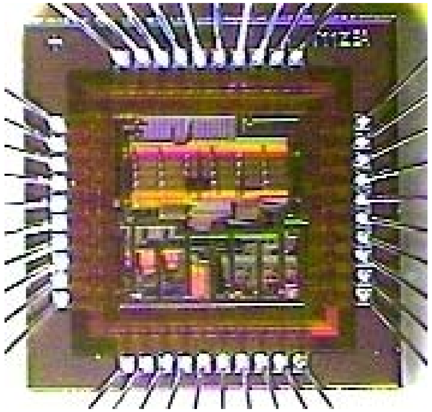
Base Band

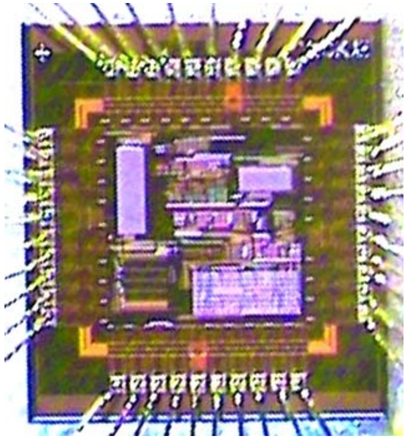
DSP
FPGA
ASICs
ASIPs

Mobile Host

Very Large Scale Integration Signal Processing Architectures

- ❒ Multi-disciplinary Process
- ❒ Mapping of Algorithms to Architectures
- ❒ Identify Datapath Blocks (Add / Mult)
- ❒ Identify Efficient Parallel Schedule
- ❒ Design & Simulate, Fabricate, Test
- ❒ FPGA for Prototype Baseband





3G Wireless Detector Circuits
Designed at Rice

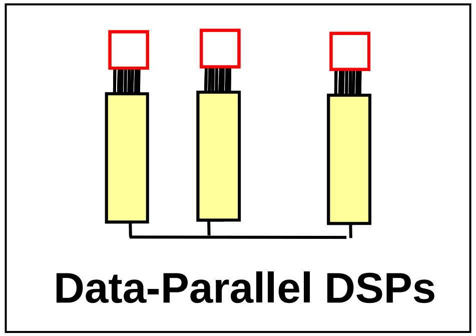
Processors in Future Wireless Systems

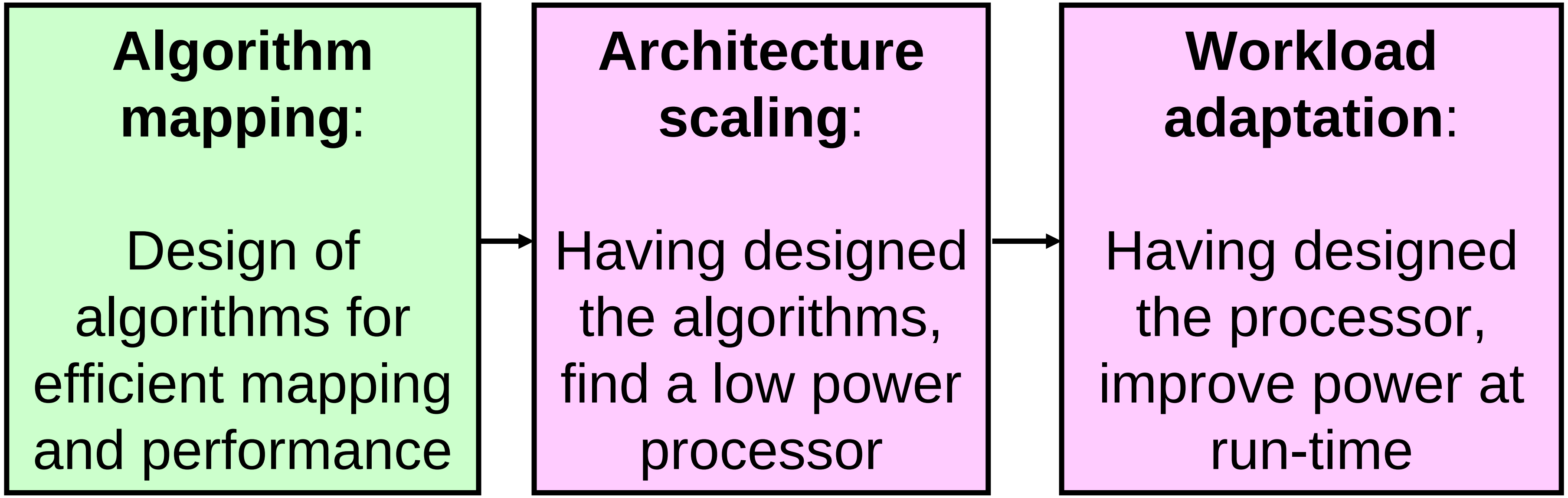
- ASIPs (Application Specific Instruction set Processors):
- Excellent Tradeoff between Efficiency of ASICs and Flexibility of DSPs
- Implementation of Special Function Units (SFUs) for Customization
- Flexible and Retargetable Compilation – Machine Description File

System Design Methodology

- Algorithm Mapping to Parallel Architectures
  - ⇒ Real-time data and sampling rates and the corresponding area and time complexities
- Configurable Mapping and Design Exploration
  - ⇒ Heterogeneous DSP and programmable application-specific instruction (ASIP) processor architectures
- Verification and Testbed Integration
  - ⇒ Prototype implementation on programmable devices and integration with RF units.

ASIP Processor Design Exploration Strategies Example





Algorithm mapping:

Design of algorithms for efficient mapping and performance

Architecture scaling:

Having designed the algorithms, find a low power processor

Workload adaptation:

Having designed the processor, improve power at run-time

Sridhar Rajagopal (Imagine) and Predrag Radosavljevic (TTA)

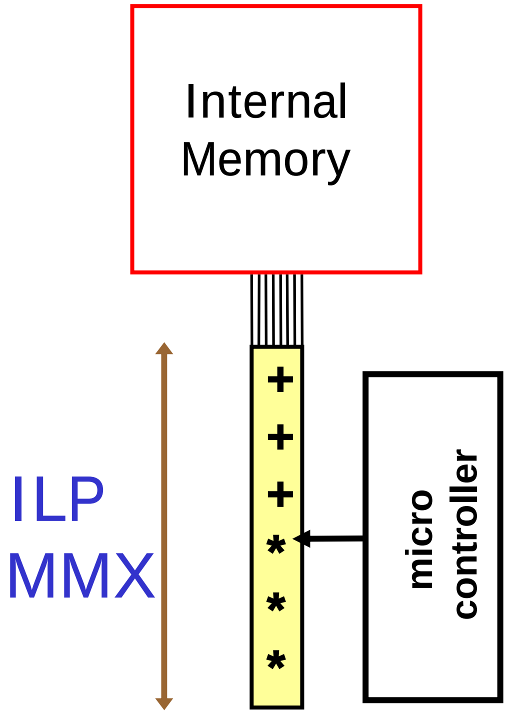
ASIP System Research Tools

- Characterized by Machine Description File and Retargetable Compiler
- VLIW – type Data Parallel Systems

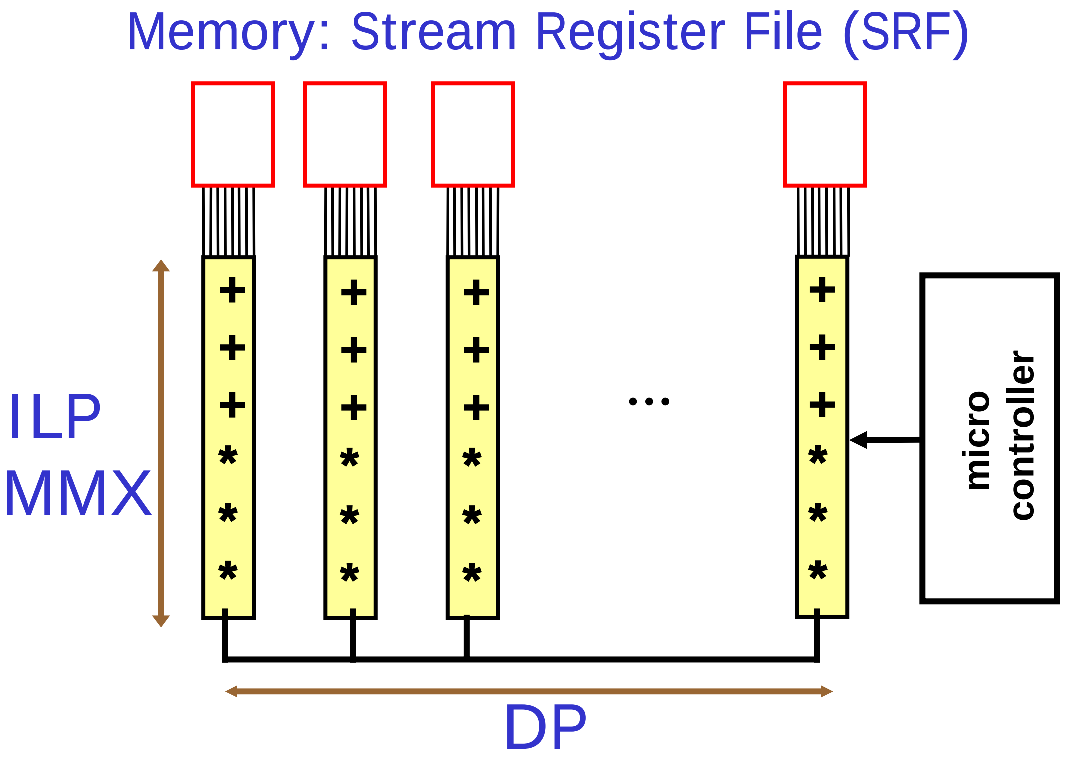
- Imagine Streaming Media Processor – MIT/Stanford

- Transport Triggered Architecture – Delft/Tampere

Stream Processors : Multi-cluster DSPs (Micro'04)



VLIW DSP
(1 cluster)

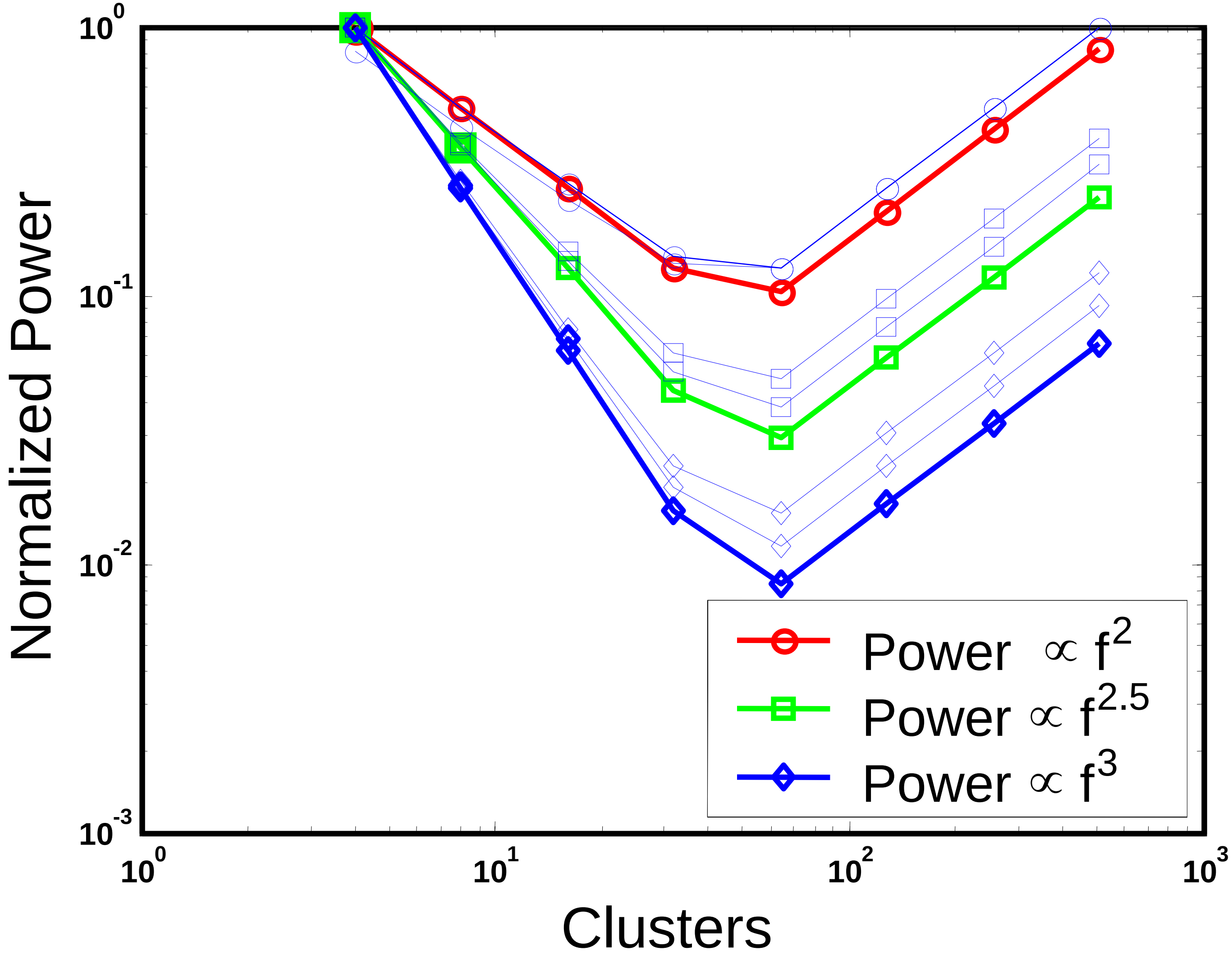


Adapt clusters to DP
Identical clusters, same operations.
Power-down unused FUs, clusters

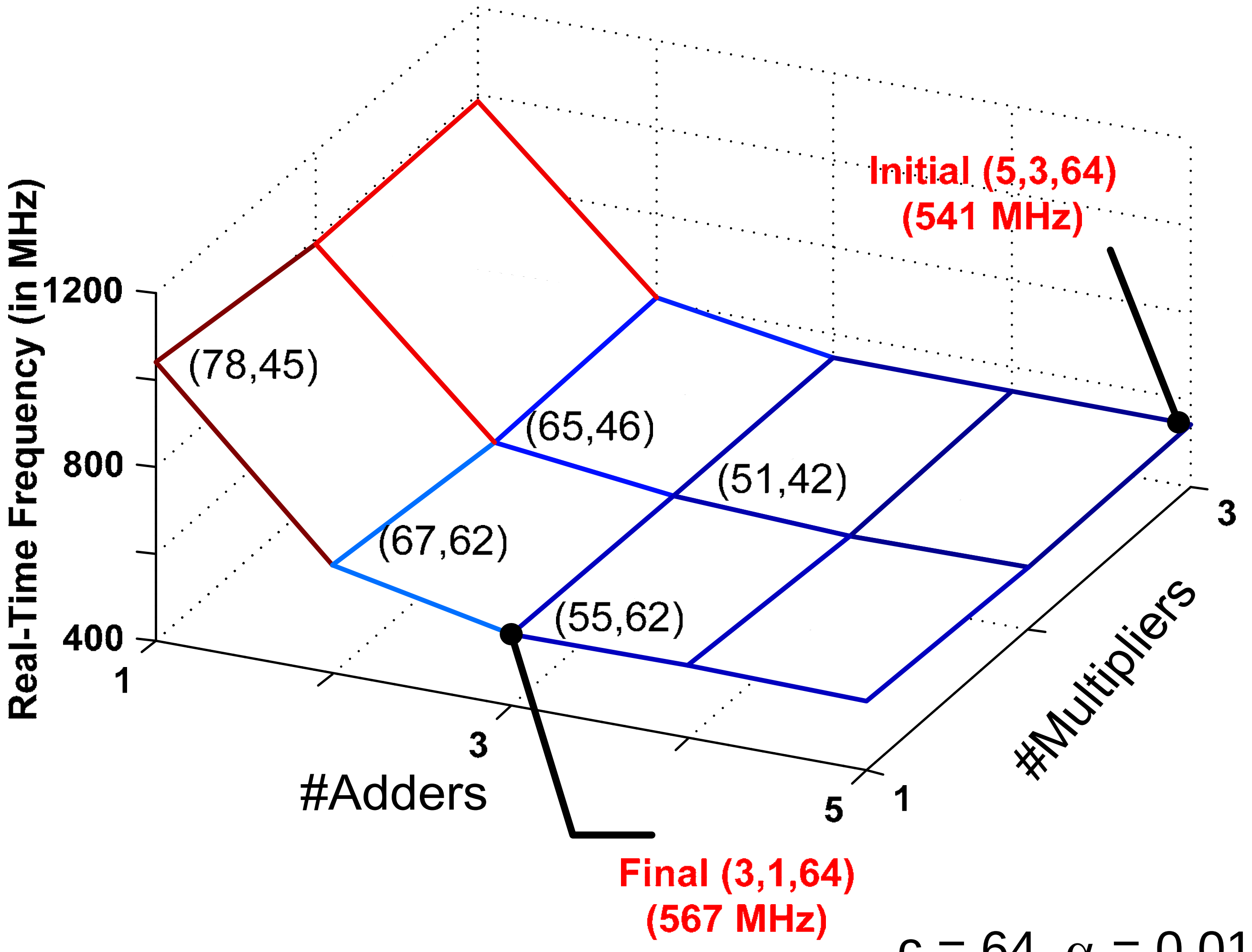
Example: 3G Algorithm Kernels Running at (a_{max},m_{max}, c_{CDP})

Algorithm	Kernel	CDP	MHz
Estimation	Correlation	32	1
	Matrix mul	32	43
	Iteration	32	1
	Transpose	512	< 1
	Matrix mul L	32	22
	Matrix mul C	32	22
Detection	Matched filter	32	71
	Interference cancellation	32	83
Decoding	Packing	256	<1
	Re-packing	64	<1
	Initialization	64	17
	Add-Compare-Select (ACS)	64	254
	Decoding output	64	23
Min. real-time frequency (a,m,c) =(5,3,512)			538 MHz

Cluster Size Relationship with Parallelism - c = 64, at 541 MHz



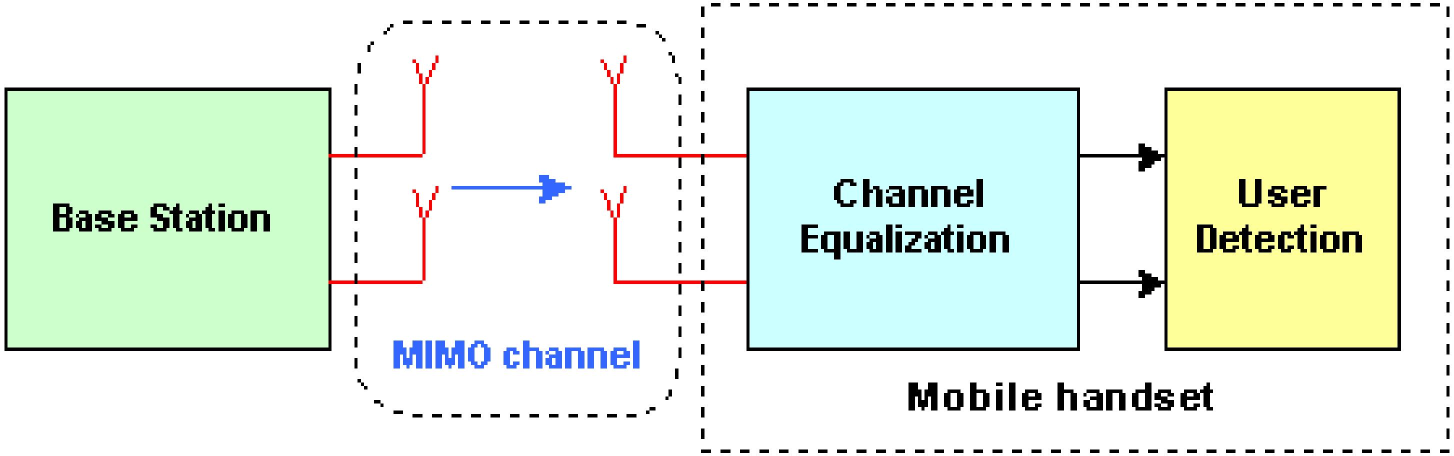
ALU Utilization (+,*) Exploration



c = 64, $\alpha = 0.01$, $\beta = 1$, p = 3

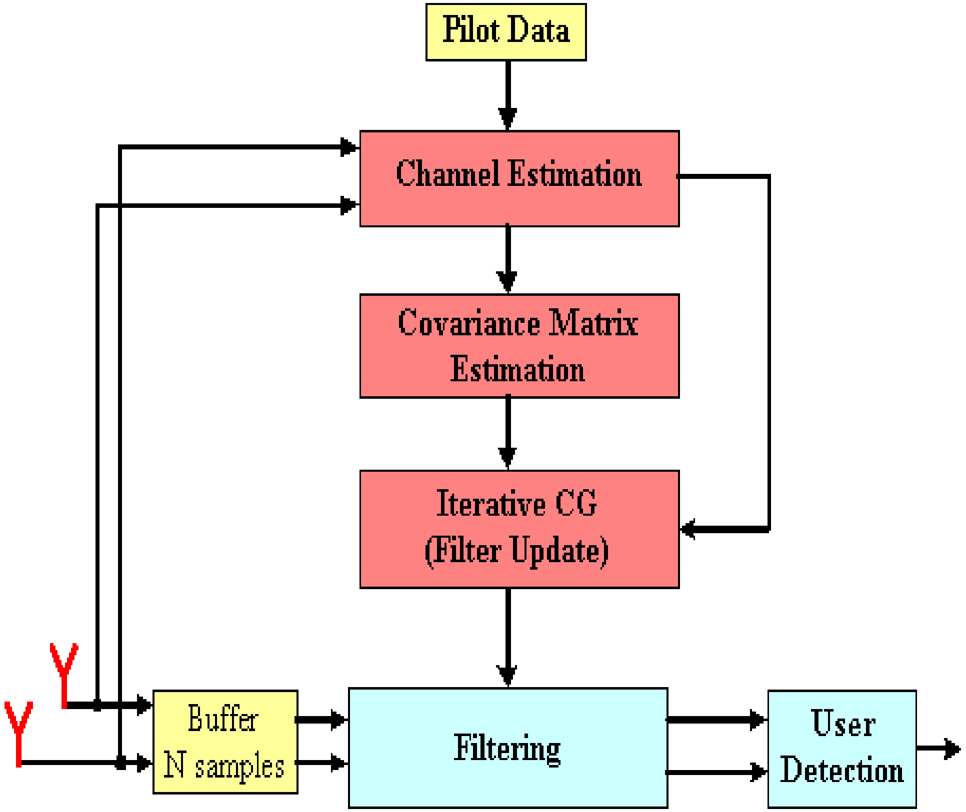
TTA Processors: HSDPA Channel Equalization (VTC'04)

- Downlink transmission in MIMO wireless system
- Linear channel equalization on the receiver side
- Physical layer of the mobile handset for 3GPP wireless standard – HSDPA application
- Programmable and customizable processor implementation



Channel Equalization
CG Algorithm and Adaptation

- Block equalization
- Latency of N samples:
  - ⇒ 4096 in slow fading
  - ⇒ 256 in fast fading
- Second order statistics
  - ⇒ Channel estimation
  - ⇒ Covariance matrix
- Modified algorithm
  - ⇒ Fast fading channels
  - ⇒ Weighted averaging
    - second order statistics

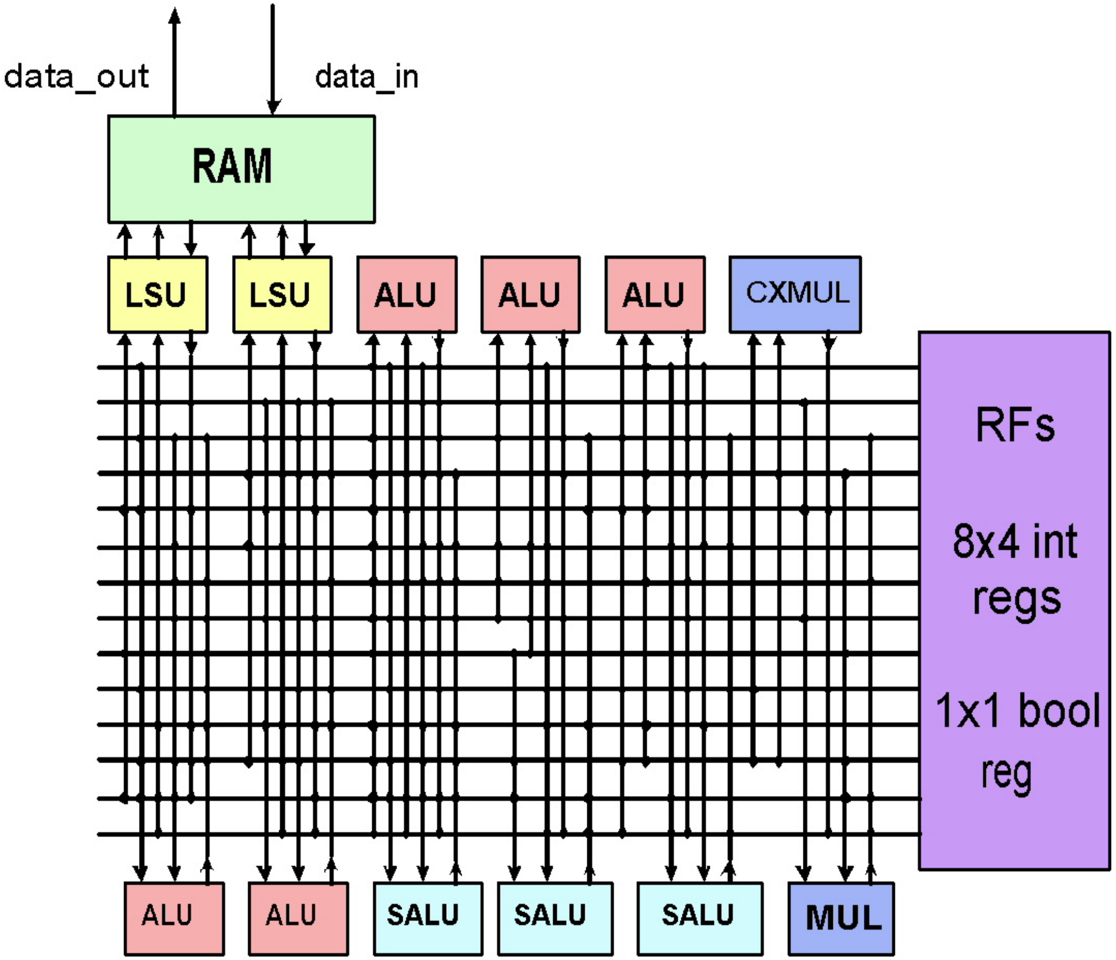


Channel equalization at the mobile handset

TTA Processor for Equalization

- Customized Processor for CG Filter Update in 2x2 Case
  - ⇒ Application-specific SFUs for equalization
- Area of approximately 76K Gates
- Flexible Design Exploration
  - ⇒ Equalization in broad range of environments
  - ⇒ Dynamic power dissipation:
    - 26 mW – 42 mW
  - ⇒ Minimum clock frequency to achieve real time:
    - 37 MHz – 104 MHz

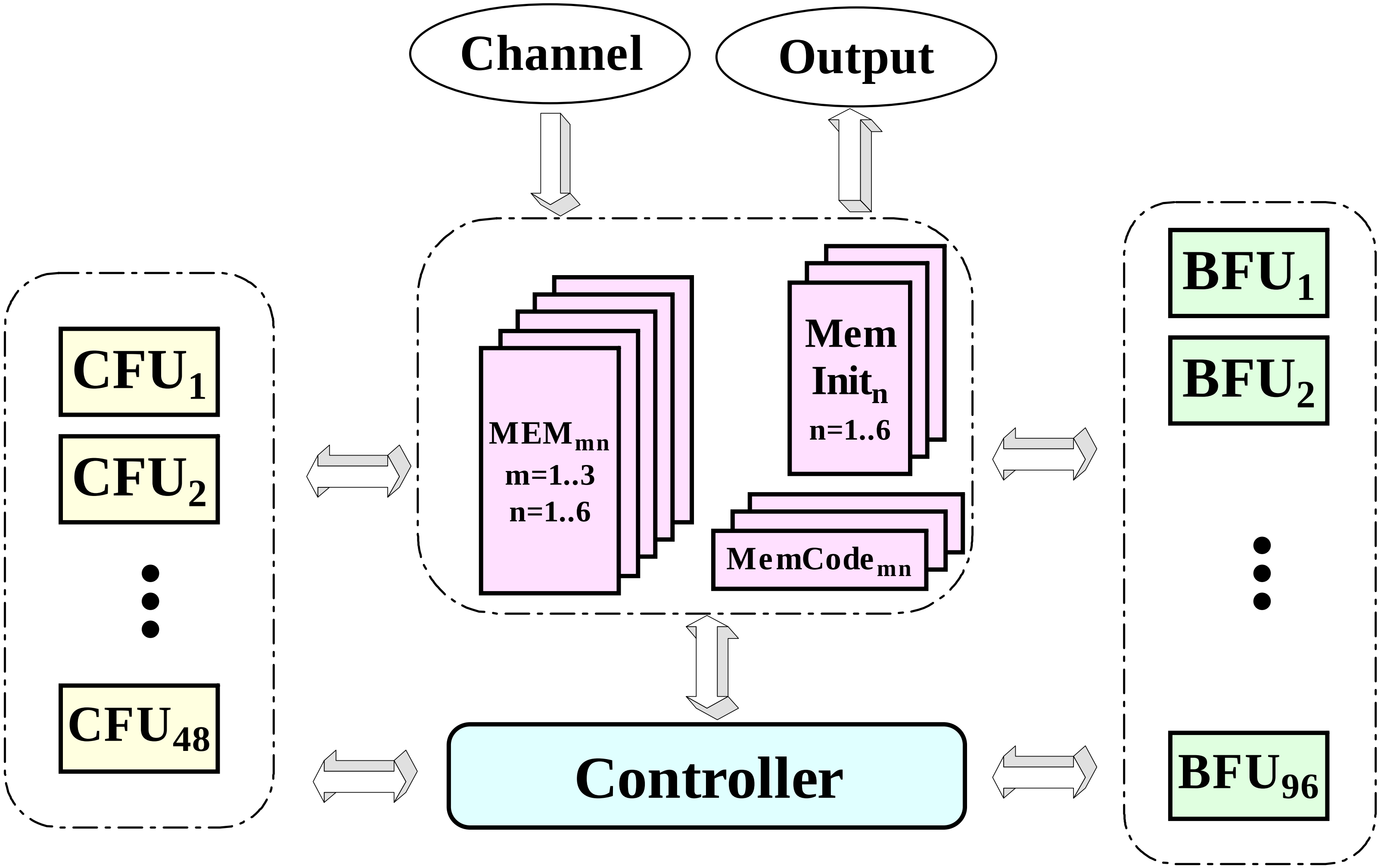
Generated TTA Processor Architecture

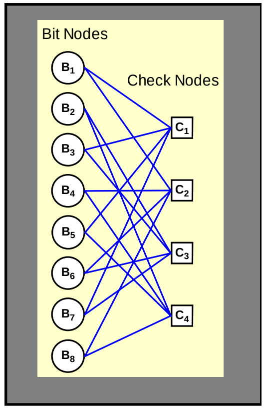


Example: LDPC Decoding - (ITCC'04)

- High Performance Decoding for Next Generation Systems
- Emerging Algorithm – Early Stages of Design and Hardware Implementation
- Unique View on Tradeoffs of BER Performance and Hardware Complexity
- Parallel Architecture Prototype in VHDL and LabVIEW FPGA to Target Flexible FPGAs

Semi-Parallel LDPC Decoder Architecture





Decoding Parameters for Architecture Analysis

- Decoding algorithm: Modified Min-Sum
- Block length: 768,1536
- Code rate: 1/2
- Structured Parity check matrix
  - ⇒ Row degree: 6
  - ⇒ Column degree: 3
- Maximum # of iterations: 20
- Message bit-length: 5 bits

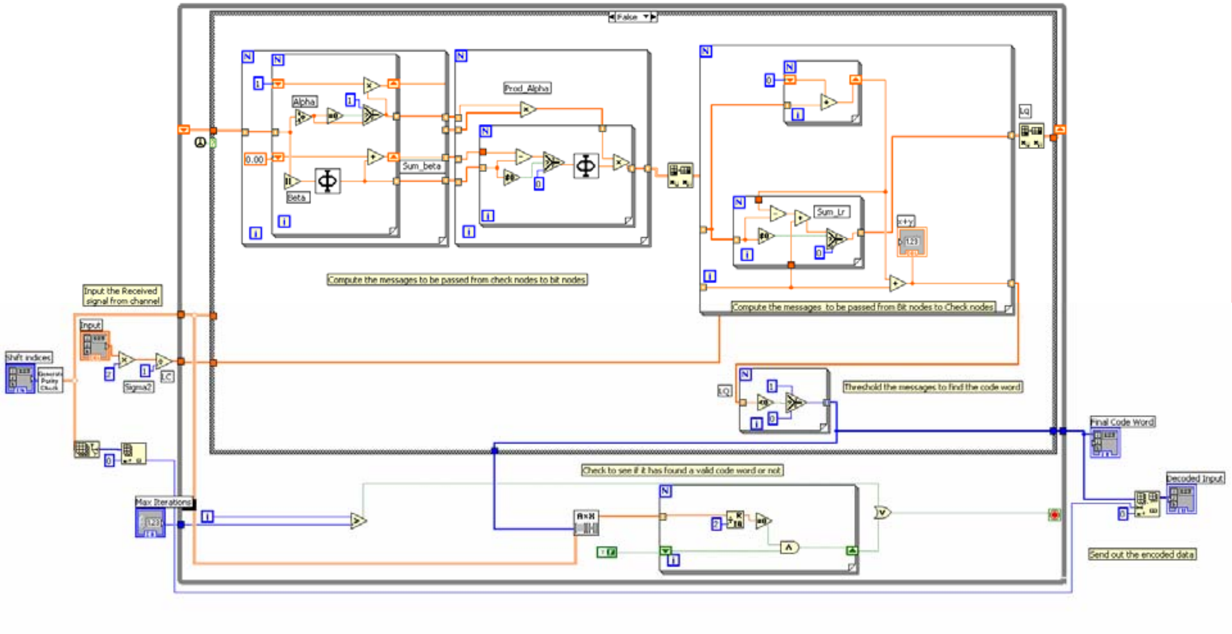
LDPC FPGA Design Statistics

- A (3,6) semi-parallel LDPC decoder has been implemented in VHDL and Using LabVIEW FPGA
- For a VirtexII-3000 FPGA

Decoder Structure	LabVIEW FPGA
Block Length	768 bits
Slices	97%
External IOBs	19%
RAMB16s	25%

LabVIEW Implementation

- Full Communication Link
- LabVIEW Host
  - ⇒ LDPC Encoder
  - ⇒ AWGN
  - ⇒ LDPC Decoder
- Co-Simulation
  - ⇒ FPGA Decoder



- Current Work: New Layered Row and Column Schedules

Testbeds: Rice University CMC Laboratory

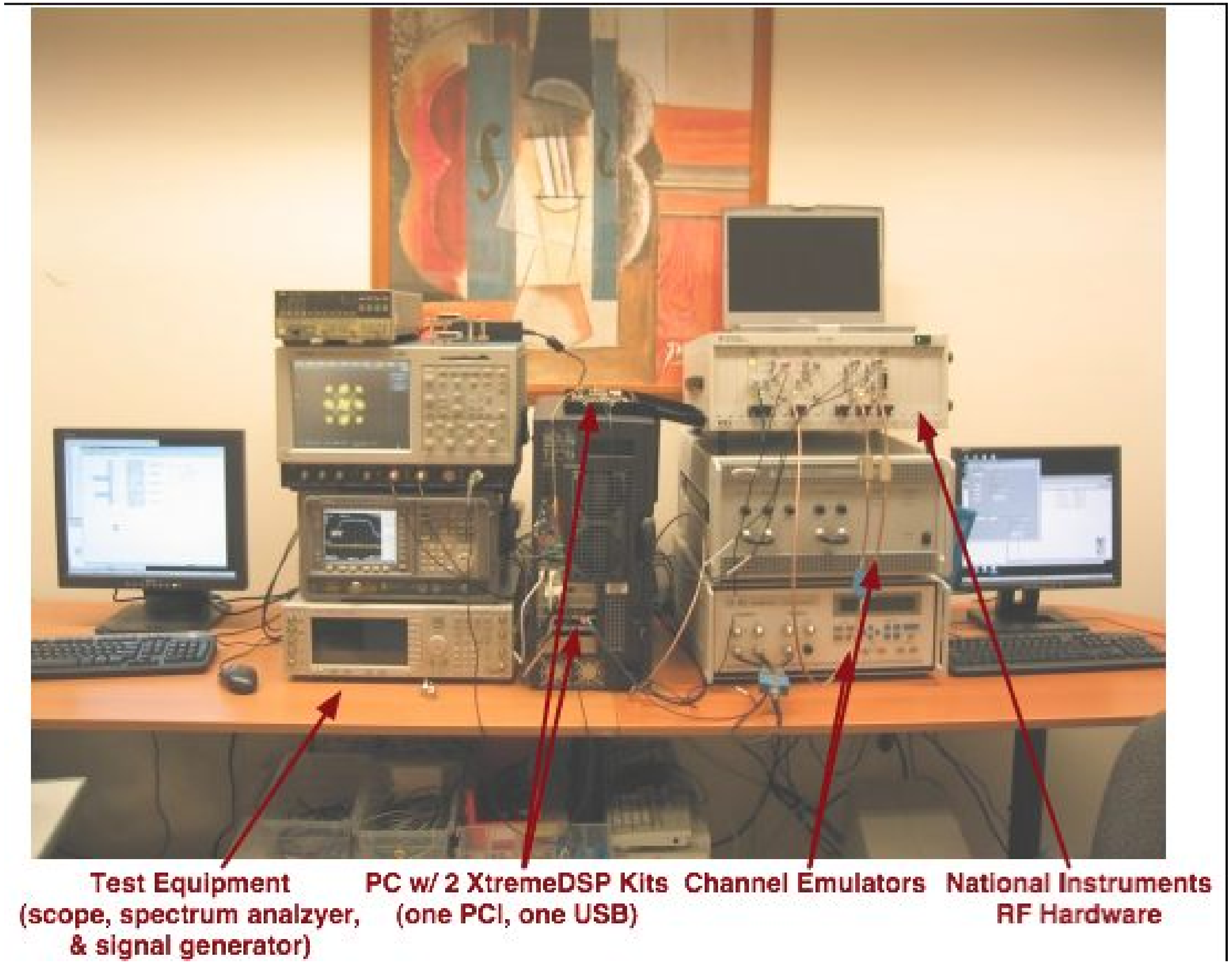
- Collaboration with TI, Nokia, National Instruments, Spirent Communications, Xilinx, and US National Science Foundation.

- Key Instruments are Channel Emulators to inject realistic channel conditions – Recorded or Simulated
- FPGA Prototype Hardware for VLSI Signal Processing for Baseband

CMC Wireless Testbed Components

- Integration of Digital Baseband, RF, and Channel Emulation
- NI LabVIEW for Control Software in First Version
- 2.4 GHz Radio Upconverters, Downconverters and Programmable RF Switch Gear
- Programmable and Reconfigurable
- Ongoing Development of Custom FPGA System for MIMO Research

CMC Testbed Hardware



Rice Transit Access Points – MIMO OFDM Testbed

- Rice Networking Group Relay Network Architecture
- 2 x 2 MIMO OFDM-based channel measurement system at 2.4 GHz
- Baseband processing and digital up and down conversion on FPGAs – Flexible waveforms
- Nallatech FPGA Kits with National Instruments radios for amplification and analog up and down conversion
- Custom FPGA and RF system based on Virtex-II Pro and Maxim 2.4 GHz radios under Development

University of Oulu 4G Lab

- Elektrobit EB4G Testbed System
- Physical 2.4 GHz RF link for MIMO Research between Elektrobit Research and CWC
  - ⇒ 1 Km Non-line of Sight
- FPGA based System with Open Architecture
  - ⇒ Core and Algorithm Research Hardware Partition
- Integrates with PropSim and PropSound
- 2 x 2 System under Development
  - ⇒ Rapid Prototyping and Experimental Verification
  - ⇒ MIMO Detectors – Extensions to LMMSE and Sphere-like Decoding

Related Testbed Efforts

- Elektrobit EB4G Research Use
  - University of Oulu
  - VTT
  - Osaka University
- UCLA / Ohio State University
- University of Texas, Austin

- Common Goals on MIMO and Beyond 3G Algorithm Research Characterization with FPGA and DSP Baseband and 2.4 GHz Radios

Summary

- Wireless Architectures - Rice Research:
  - ⇒ VLSI Signal Processing Architectures
    - Channel Estimation and Equalization
    - Multi-user Detection
    - Decoding
  - ⇒ Programmable and Configurable ASIPs
    - Imagine, TTA
  - ⇒ Development of CMC Wireless Testbed
- Rice – CWC Research Interaction
  - ⇒ CWC Postgraduate Course
  - ⇒ Beyond 3G Research and Elektrobit EB4G Testbed